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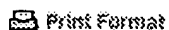
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Takashima, D.; Shuto, S.; Kunishima, I.; Takenaka, H.; Oowaki, Y.; Tanaka, S.;  
Solid-State Circuits, IEEE Journal of , Volume: 34 , Issue: 11 , Nov. 1999  
Pages:1557 - 1563

[Abstract] [PDF Full-Text (340 KB)] IEEE JNL

2 High-density chain ferroelectric random access memory (chain FRAM)

Takashima, D.; Kunishima, I.;  
Solid-State Circuits, IEEE Journal of , Volume: 33 , Issue: 5 , May 1998  
Pages:787 - 792

[Abstract] [PDF Full-Text (140 KB)] IEEE JNL

3 A sub-40 ns random-access chain FRAM architecture with a 768 cell-plate-line drive

Takashima, D.; Shuto, S.; Kunishima, I.; Takenaka, H.; Oowaki, Y.; Tanaka, S.;  
Solid-State Circuits Conference, 1999. Digest of Technical Papers. ISSCC. 1999  
IEEE International , 15-17 Feb. 1999  
Pages:102 - 103

[Abstract] [PDF Full-Text (300 KB)] IEEE CNF

4 Gain cell block architecture for gigabit-scale chain ferroelectric RAM

Takashima, D.; Oowaki, Y.; Kunishima, I.;  
VLSI Circuits, 1999. Digest of Technical Papers. 1999 Symposium on , 17-19 June 1999